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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,230	KELLY ET AL.	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,14-17,19-21,23 and 27-29* is/are rejected.

7)☒ Claim(s) *6-13,18,22 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Appeal's Brief for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Fang (U.S. Patent 6,084,779).

As to claim 1, Fang discloses a printed circuit board (10) as shown in figure 5 comprising:

a printed circuit board substrate (multiplayer PCB 12, 14, 16, 18, 20, 22, and 24)

a signal layer (a signal layer 12 is described in column 3, lines 62-67 in the embodiment of figure 1, but the layer 12 is the same structure in another embodiment of figure 5), supported by the printed circuit board substrate (multiplayer PCB), the signal layer (12) comprising traces (not shown) to communicate signals not associated with regulated supply voltage (because the traces of the signal layer 12 are provided as

signal lines or patterns connected to a component formed on the PCB and not used to provide power or ground for purpose); and

a supply voltage plane (power path 46) supported by the substrate and embedded in the signal layer (12) to supply power to multiple supply pins of a component (decoupling capacitor 52) mounted to the printed circuit board (10).

As to claim 2, Fang further discloses a supply voltage plane layer (14), see figure 5b, separate from the signal layer (12).

As to claim 14, Fang discloses the PCB as shown in figure 5b wherein the supply voltage (of the supply voltage plane 46) that reduces and inductance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-5, 20-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang ('779) in view of Kan (U.S. Patent 6,265,952).

As to claims 3-5, Fang discloses a printed circuit board (10) as shown in figure 5 and 6 comprising:

a printed circuit board substrate (multiplayer PCB 12, 14, 16, 18, 20, 22, and 24)

a signal layer (a signal layer 12 is described in column 3, lines 62-67 in the embodiment of figure 1, but the layer 12 is the same structure in another embodiment of

figure 5), supported by the printed circuit board substrate (multiplayer PCB), the signal layer (12) comprising traces (not shown) to communicate signals not associated with regulated supply voltage (because the traces of the signal layer 12 are provided as signal lines or patterns connected to a component formed on the PCB and not used to provide power or ground for purpose); and

a supply voltage plane (power path 46) supported by the substrate and embedded in the signal layer (12) to supply power to a component (IC chip, column 4, line 14), see figure 6, mounted to the printed circuit board (10), the IC chip is a surface mounted component having a main body connected right on a region where the supply voltage plane embedded in the signal layer.

Fang does not explicitly disclose the IC chip having supply voltage pins, it is a surface mounted. Kan shows an electrical component (50) having supply voltage pins (55) having an outer boundary connected to a PCB (3), see column 3, lines 28-35.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a component having supply voltage pins in the PCB of Fang instead of the surface mounted IC chip, as taught by Kan, because the pins of the component are directly connected to each of inner-layers of the PCB for reducing noise without using bonding pads, and the wire-bonded is easy to break during delivery that may causes short circuit for the user.

With respect to claims 20-21, 23, Fang discloses a method for a component (IC chip, column 4, line 14) mounted on a PCB (10) comprising:

embedding an associated supply voltage plane (46) in a signal layer (12) of the PCB (10) to provide power to the component (IC), the signal layer being used to communicate and associate with the component (IC),

coupling the supply voltage plane (46) embedded in the signal layer (12) to a supply voltage plane layer (14 or 20) separately from the signal layer (12), and locating the supply voltage plane underneath the component wherein the component is mounted on the top of the signal layer (12).

Fang does not explicitly disclose the IC chip is a high frequency component. Kan shows a high frequency component (50), see column 3, lines 28-30) formed on a PCB (3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a high frequency component to replace the IC chip in the PCB of Fang, as taught by Kan, for the purpose of operating high frequency signals without excessive noise.

6. Claims 15-17, 19, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkman ('113) in view of Kan (U.S. Patent 6,265,952).

As to claims 15-17, 19, 27-29, Kirkman discloses a printed circuit board (42, see figures 2-3) and its method comprising:

a printed circuit board substrate (100; 200; 300, 80, 82, 84, and 86), see the sketch on an attaching paper;

a supply voltage plane layer (84-see figure 3) supported by the substrate to communicate a supply voltage (not show); and

a ground plane (90) supported by the substrate embedded in the supply voltage plane layer (84) and coupled to a ground plane layer (82) separately from the supply voltage plane layer (84), the ground plane (90) has an outer boundary, locates directly below a component (die 62), and provides ground connections (by ground vias) to the component (62) mounted on the printed circuit board.

Kirkman discloses a wire-bonded component but does not disclose a high frequency component having a multiple pins connected to the PCB. Kan shows a PCB (3, see column 3, line 15, in figure 1), comprising a high frequency component (50) having multiple pins (55) mounted to the PCB instead of wire-bonded.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a high frequency component having multiple pins connected to the PCB in the PCB of Kirkman instead of wire-bonded component, as taught by Kan, because the pins are directly connected to each of inner-layers of the PCB for reducing noise without using bonding pads, and the wire-bonded is easy to break during delivery that may causes short circuit for the user.

Allowable Subject Matter

7. Claims 6-13, 18, 22, and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 6 and 24, the references cited, for example, Kirkman (U.S. Patent 6,064,113) discloses a power and ground plane (84) having a ground portion (90) embedded in the plane (84), Buffet et al. (U.S. Patent 6,477,057) discloses a shielding layer (or ground) embedded in a power plane (211). However, they do not discloses or render obvious in combination of the PCB of Fang (U.S. Patent 6,084,779) having a voltage supply plane layer different from the signal layer, the supply voltage plane layer comprising an embedded ground plane to provide ground connection for the signal layer.

Claim 18 is allowable because Kirkman does not disclose the ground connections that are associated with electrical devices connected to the component. There is no suggestion to modify these references to include these limitations.

Claim 22 is allowable because the references cited do not disclose the step of coupling an inductive element between at least one of the supply voltage plane and the supply voltage plane layer.

Response to Arguments

13. Applicant's Appeal Brief filed 03/19/2004 have been fully considered are persuasive.

Applicant argues:

(a) The examiner fails to establish a prima facie case of obviousness for claims 1-29 for at least the reason that the examiner fails to show where the prior art contains the alleged suggestion or motivation to combine Kirkman and Nuxoll.

Examiner agrees the combination of Kirkman in view of Nuxoll does not read on claims 1-29

However, applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection as explained above.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kakimoto et al., Mazumder, Ball et al., and Buffet et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
June 21, 2004.

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